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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/028,429	12/28/2001	Koichi Hashimoto	107317-00039	4380

4372 7590 02/12/2004

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EXAMINER	
NGUYEN, KHIEM D	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 02/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/028,429	HASHIMOTO ET AL.	
	Examiner	Art Unit	
	Khiem D Nguyen	2823	

-- Th MAILING DATE of this communication appears on th cover she t with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 November 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13,14 and 16-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13,14 and 16-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on November 17th, 2003 has been entered. A new rejection is made as set forth in this Office Action. Claims (13, 14, and 16-19) are pending in the application.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 13 and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by Owada et al. (U.S. Patent 5,220,199).

In re claim 13, **Owada** discloses a method of manufacturing a semiconductor device for forming a plurality of first wiring patterns and a second wiring pattern at the same time on a same level (col. 5, line 8 to col. 7, line 25 and **FIGS. 1-10**), the first wiring patterns **(FIG. 4: 22a-22d)** being connected to a gate electrode on a gate insulating film formed on a semiconductor region (col. 6, lines 20-37), and the second

wiring pattern **(FIG. 4: 3)** (power source wiring) (col. 7, lines 13-25) being connected to the semiconductor region, wherein in patterning the first and second wiring patterns, a dummy wiring pattern **(FIG. 4: 8)** electrically separated from and placed between the first and second wiring patterns on the same level is left unetched (col. 6, line 57 to col. 7, line 2), the dummy wiring pattern not positively serving as any element in a circuit of the semiconductor device (col. 5, lines 25-49).

In re claim 14, **Owada** discloses wherein the spaces between the dummy pattern **(FIG. 4: 8)** and the first **(FIG. 4: 22a-22d)**, and second wiring patterns **(FIG. 4: 3)** are set generally equal to a minimum pattern space of the first, and second wiring patterns **(FIGS. 4 and 7)**.

2. Claims 16-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Owada et al. (U.S. Patent 5,220,199).

In re claim 16, **Owada** discloses a method of manufacturing a semiconductor device for forming a plurality of first wiring patterns and a second wiring pattern at the same time on a same level (col. 5, line 8 to col. 7, line 25 and **FIGS. 1-10**), the first wiring patterns **(FIG. 4: 22a-22d)** each being connected to a gate electrode on a gate insulating film formed on a semiconductor region (col. 6, lines 20-37), and the second wiring pattern **(FIG. 4: 3)** (power source wiring) (col. 7, lines 13-25) being connected to the semiconductor region, wherein in patterning the first and second wiring patterns, at least one dummy wiring pattern **(FIG. 4: 8)** which is electrically separated from and placed between the first and second wiring patterns on the same level is left unetched

(col. 6, line 57 to col. 7, line 2), the dummy wiring pattern not positively serving as any element in a circuit of the semiconductor device (col. 5, lines 25-49).

In re claim 17, **Owada** discloses wherein the spaces between each adjacent pair of wiring patterns are set equal to a minimum wiring pattern space of the first **(FIG. 4: 22a-22d)** and second wiring patterns **(FIG. 4: 3) (FIGS. 4 and 7)**.

In re claim 18, **Owada** discloses a method according to claim 16, further comprising a third wiring pattern **(FIG. 4: 7a-d)** (signal wirings) (col. 5, lines 8-24) between the first wiring pattern **(FIG. 4: 22a-22d)** and second wiring pattern **(FIG. 4: 3)**, the third wiring pattern being connected in the circuit of the semiconductor device, wherein the at least one dummy wiring pattern **(FIG. 4: 8)** includes at least one dummy wiring pattern in each of the spaces between the third wiring pattern and the first and second wiring patterns **(FIGS. 4 and 7)**.

In re claim 19, **Owada** discloses wherein the spaces between each adjacent pair of wiring patterns are set equal to a minimum wiring pattern space of the first **(FIG. 4: 22a-22d)** and second wiring patterns **(FIG. 4: 3) (FIGS. 4 and 7)**.

Response to Amendment

Response to Arguments

3. In response to Applicant's argument that Matsuoka fails to teach and/or suggest a dummy wiring pattern electrically separated from and placed between the first and second wiring patterns on the same level and is left unetched wherein the dummy wiring pattern is not positively serving as any element in a circuit of the semiconductor device, examiner respectfully disagree. Applicants are directed to pages 2-3 in the Office Action where the

newly discovered reference Owada et al. (U.S. Patent 5,220,199) discloses a method of manufacturing a semiconductor device for forming a plurality of first wiring patterns and a second wiring pattern at the same time on a same level (col. 5, line 8 to col. 7, line 25 and FIGS. 1-10), the first wiring patterns (FIG. 4: 22a-22d) being connected to a gate electrode on a gate insulating film formed on a semiconductor region (col. 6, lines 20-37), and the second wiring pattern (FIG. 4: 3) (power source wiring) (col. 7, lines 13-25) being connected to the semiconductor region, wherein in patterning the first and second wiring patterns, a dummy wiring pattern (FIG. 4: 8) electrically separated from and placed between the first and second wiring patterns on the same level is left unetched (col. 6, line 57 to col. 7, line 2), the dummy wiring pattern not positively serving as any element in a circuit of the semiconductor device (col. 5, lines 25-49).

For this reason, examiner holds the rejection proper.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D Nguyen whose telephone number is (571) 272-1985. The examiner can normally be reached on Monday-Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3432 for regular communications and (703) 305-3432 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

K.N.
February 2, 2004

W. DAVID COLEMAN
PRIMARY EXAMINER